REMARKS

The Examiner's Action mailed on April 15, 2005 has been received and its contents carefully considered.

Claims 1-13 are pending in this application. New claims 14-20 are added herein. Original claim 1 and new claim 14 are independent claims.

In the Action, claims 1-10 are rejected under 35 USC 102 as being anticipated by Balachandran et al. (U.S. Patent No. 6618830). The rejection is respectfully traversed.

Regarding claim 1, the Examiner asserts that the nets in circuit 20 of Balachandran correspond to the connections between scan cells recited in claim 1, and that they are formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer, as disclosed in col. 1, lines 14-47 and 52-61, and col. 6, lines 15-30 and 50-63. However, as disclosed in col. 6, lines 15-30, Balachandran teaches that the nets in circuit 20 are identifiable based on a coordinate map corresponding to the physical dimensions of a particular circuit 20. A particular net may be identifiable based on its length, width and depth or the horizontal and vertical dimensions and position of the net of circuit 20. Thus, Balachandran teaches that the particular net may be identifiable based on its physical dimensions and position rather than **formed according to a layout constraint with a minimum dimension for an assigned routing layer**.

Further, as disclosed in col. 6, lines 50-63, to which the Examiner also makes reference, Balachandran teaches only design rules include restrictions for particular circuit 20. For example, the design rules or restrictions specify that the metal line pitch or distance between the center of one metal lead or metallization layer and a adjacent metal lead or metallization layer are no less than 1.5 microns in length. Thus, Balachandran only teaches restrictions to limit space between one metal lead or metallization layer and an adjacent metal lead or metallization layer rather than **forming a connection according to a layout constraint with a minimum dimension for an assigned routing layer**.

Therefore, it is submitted that contrary to the Examiner's position, Balachandran fails to teach or suggest an important limitation recited in claim 1, namely, that each connection is **formed according to a layout constraint with a minimum dimension** provided by design rules **for an assigned routing layer**. The Applicants believe that this

significant difference between Balachandran and the claimed invention reflects the fact that Balachandran is directed to a system for generating a pruned diagnostic list of potential bridging faults in a circuit. The system includes a pattern generator operable to generate test patterns for testing the circuit and a tester in communication with the pattern generator that is operable to apply the test patterns to the circuit and generate a plurality of resulting test vectors (see Abstract). A bridging fault is one that involves more than one net in the circuit. A bridging fault may involve, for example, two metal leads within a particular circuit layer or adjacent circuit layers that are shorted, causing a fault that may not be easily detected or diagnosed using the conventional stuck-at fault model of testing (col. 1, lines 52-58). In general, the system in Balachandran generates diagnostic information using conventional stuck-at fault testing, converts the diagnostic information into refined diagnostic information suggesting possible bridging faults, and then prunes such refining diagnostic information in response to the physical data associated with the circuit 20 (col. 3, lines 42-47). Based on that physical data, a pruning module generates adjacency criteria specific to particular circuit 20 and applies these criteria to the refined diagnostic information to identify the most probable bridging faults (col. 6, lines 35-40). Thus, the focus in Balachandran is on identifying circuit faults that probably result from the physical proximity of two nets in the circuit.

By contrast, the present invention is directed to an integrated circuit capable of locating failure process layers on a chip. This objective is accomplished by providing an integrated circuit having a substrate with a scan chain disposed thereon. The scan chain has scan cells connected to form a series chain. Each connection between scan cells is formed according to a layout constraint with minimum dimensions provided by design rules for an assigned routing layer. Since the connection in the assigned routing layer is constrained to a minimum, the scan chain is vulnerable to variations in processes relevant to the assigned routing layer. This scan chain makes it easier to identify those processes causing low yield rates (application page 2, lines 1-12). Given the significant differences in purpose, it is not surprising that Balachandran and the present invention have significant differences in structure.

Accordingly, it is respectfully submitted that claim 1 patentably distinguishes over the applied prior art. Inasmuch as claims 2-10 depend from claim 1, it is the Applicants belief that the §102 rejection of 1-10 should also be withdrawn.

Claims 11-13 are rejected under 35 USC 103 as being unpatentable over Balachandran in view of Barth et al. (U.S. Patent No. 6233184). The rejection is respectfully traversed.

To establish a prima facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine referenced teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2142.

With respect to claims 11-13 the Examiner acknowledges that Balachandran fails to disclose an integrated circuit on a chip further comprising an auxiliary routing net positioned in parallel beside the scan chain to replace one of the connections in the scan chain, and the auxiliary routing net does not function when the scan chain is originally formed. To cure this deficiency in Balachandran, the Examiner points to the membrane ribbon connectors 31 in Barth as corresponding to the recited "auxiliary routing net positioned in parallel beside the scan chain, the auxiliary routing net has metal lines of different lengths (to replace one or more of the connections in the scan chain), and the auxiliary routing net does not function when the scan chain is originally formed" (col. 1, lines 5-10; col. 4 lines, 4-64; col. 8 lines 19-67; col. 9, lines 1-6; col. 12, lines 48-65). The Examiner argues that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ Barth's teaching regarding an integrated circuit on a chip further comprising an auxiliary routing net, and use it in Balachandran's invention to replace failing cells, word lines or bit lines by disconnecting shorted cells connecting good cells into chains, thereby improving wafer burn-in scheme that permits parallel test and burn of the chips on a waiver before dicing without a costly glass ceramic interface.

The Applicants respectfully disagree. What the referenced text in Barth discloses is an invention that provides full test and burn-in by attaching a membrane to a wafer having

self test engines (col. 4, lines 41-42). The membrane 20 shown in Fig. 3a of Barth has at least one wiring level 22 extending on insulation layer 24 and is electrically connected and mechanically bonded to wafer 26 (col. 5, lines 42-45). Barth discloses that as a first step in testing, membrane 20 is attached to wafer 26 and all test engines 29 and power and ground of all chips are electrically connected to membrane 20 (col. 6, lines 8-10). As shown in Figs. 3b and 3c, connections between wafer 26 (including chips 28 and test engines 29) and membrane third 20 are preferably made with a thermal compression bonding tool that cuts one side of wire 22 extending over opening or via 30 in membrane 20 and makes thermal compression bonds between ribbon connector 31 and chip pad 32 (col. 6, lines 20-25). As shown in Fig. 3e, membrane ribbon connectors 31 can be cut and removed to open contact and disconnect chips 28 that short during test or burn-in (column 6 lines 48-50).

Thus, Barth fails in at least two significant respects to disclose the features recited in claim 11. First, the "auxiliary routing net" to which the Examiner points is not part of the integrated circuit, as claim 11 requires, but rather part of a contacting membrane that is attached to the wafer after fabrication to facilitate test or burn-in, and subsequently removed. Second, contrary to requirements of claim 11, the "auxiliary routing net" in Barth does in fact function when the membrane is attached and connected to the wafer, with at least some of the chips 28 and test engines 29 being initially connected.

Further, Barth does not address the basic deficiency in Balachandran discussed above, namely, failure to meet the requirement that each connection between scan cells is formed according to a layout constraint with a minimum dimension provided by design rules for an assigned routing layer. Barth, in fact, fails to disclose that the chip under test includes any scan cells, or suggest in any way that its technique for connecting and/or disconnecting chips might be advantageous in bypassing the connections in a scan chain.

Accordingly, it is respectfully submitted that the prior art lacks the necessary suggestion or motivation for the combination proposed by the Examiner, that the references fail to disclose all the elements of the claimed invention, and that even if the teachings of the references were combined, the result would not produce the claimed invention. For at least the forgoing reasons, the applicants believe that claims 11-13 patentably distinguish over the applied prior art references, whether considered individually or in combination.

New claims 14-20 are added to recite the invention in a somewhat different manner. The Applicants believe that claims 14-20 also patentably distinguish over the applied prior art.

In summary, it is submitted that this application, with original claims 1-13 and new claims 14-20 is in condition for allowance. Notice of allowance and the passing of this application to issue, are earnestly solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

July 14, 2005
Date

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